

Application No. 10/762,658  
Filed: January 22, 2004  
TC Art Unit: 2814  
Confirmation No.: 5151

AMENDMENT TO THE CLAIMS

1. (Currently Amended) A transistor device comprising:
  - a source;
  - a drain;
  - a gate; and
  - a hole metal channel having a thickness of less than 5 nm  
with carriers controlled by the gate.
2. (Original) The device of Claim 1 further comprising an insulating layer and a gate insulator, the metal channel being positioned between the gate insulator and the insulating layer.
3. (Original) The device of Claim 1 further comprising a silicon substrate.
4. (Original) The device of Claim 1 wherein the metal channel comprises a continuous thin conductive film having a thickness less than 5 nm.
5. (Original) The device of Claim 1 wherein the metal channel has a thickness in a range of 0.2 to 3 nm.
6. (Original) The device of Claim 1 wherein the transistor comprises an enhancement mode device.
7. (Original) The device of Claim 1 wherein the transistor comprises a depletion mode device.
8. (Currently Amended) A field effect transistor device comprising:

-2-

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Application No. 10/762,658

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a an n-type metal channel formed over an insulator;  
a source including a p-type material and a drain including a  
p-type material; and  
a gate and a gate insulator formed over the channel, the gate  
controlling carriers in the channel.

9. (Original) The device of Claim 8 wherein the insulator further comprises an insulating layer over a substrate, the metal channel being positioned between the gate and the insulating layer and the gate insulator being positioned under the gate and over the metal channel.

10. (Original) The device of Claim 8 further comprising a silicon substrate.

11. (Original) The device of Claim 8 wherein the metal channel comprises a continuous thin conductive film having a thickness less than 5 nm.

12. (Original) The device of Claim 8 wherein the device further comprises a complementary transistor device.

13. (Original) The device of Claim 8 further comprising an encapsulation layer.

14. (Original) The device of Claim 8 wherein the metal channel has a length in a range of 5 nm to 50 nm and a width in a range of 50 nm to 500 nm.

Application No. 10/762,658  
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TC Art Unit: 2814  
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15. (Original) The device of Claim 8 wherein the channel comprises a plurality of layers.
16. (New) The device of Claim 1 wherein a type of carriers within the metal channel is controlled by the gate.
17. (New) The device of Claim 1 wherein the source comprises a p-type metal and the drain comprises a p-type metal, and wherein the metal channel is a p-type metal that is sufficiently thin that the number of carriers within the metal channel can be controlled by a gate to form a p-channel depletion-mode device.
18. (New) The device of Claim 1 wherein the source comprises an n-type metal and the drain comprises an n-type metal; and wherein the metal channel comprises a p-type metal such that an n-type inversion layer is formed on the p-type metal upon application of sufficient positive gate voltage to form an n-channel enhancement-mode device.
19. (New) The device of Claim 1 wherein the device further comprises a transistor of opposite conductivity type on a common substrate to form a complementary circuit.
20. (New) The device of Claim 1 wherein the channel comprises a plurality of layers.
21. (New) The device of Claim 1 wherein the metal channel comprises a metal alloy, doped metal, metal silicide, metal salicide or metal nitride.
22. (New) The device of claim 8, further comprising a p-type inversion layer.

-4-

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Application No. 10/762,658

Filed: January 22, 2004

TC Art Unit: 2814

Confirmation No.: 5151

23. (New) The device of claim 8, wherein a p-type inversion layer is formed on the n-type metal upon application of a negative gate voltage.

24. (New) The device of Claim 8 wherein the metal channel comprises a metal alloy, doped metal, metal silicide, metal salicide or metal nitride.

25. (New) The device of claim 23, wherein a thickness of the n-metal layer is greater than a thickness of the p-type inversion layer.

26. (New) The device of claim 23 wherein the p-type inversion layer is on a first side of the n-type metal to form a p-channel enhancement-mode device.

27. (New) A method of producing a field effect transistor, comprising:

forming a metal channel over a substrate;

depositing a gate insulator over the metal channel;

forming a gate over the gate insulator;

forming a source contact, a gate contact and a drain contact;

applying appropriate voltage to the gate to form an inversion layer of opposite conductivity type on the metal channel.

28. (New) A method of producing a complementary transistor integrated circuit, comprising:

forming at least two metal channels over an insulator, at least one metal channel being formed from an electron metal and at least one metal channel is formed from a hole metal;

depositing a gate insulator over each metal channel;

forming a gate over each gate insulator;

Application No. 10/762,658  
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TC Art Unit: 2814  
Confirmation No.: 5151

forming a source contact, a gate contact, and a drain contact for each device; and

each metal channel having a thickness such that a number of carriers within the metal channel can be controlled by a gate.

29. (New) The method of Claim 28 further comprising forming the insulator over a substrate.

30. (New) The method of Claim 29 further comprising forming the device over a silicon substrate.

31. (New) The method of Claim 28 further comprising forming each metal channel by depositing a continuous conductive film having a thickness less than 5 nm.

32. (New) The method of Claim 28 further comprising depositing an encapsulation layer.

33. (New) The method of Claim 28 further comprising forming metal channels have a length in a range of 5 nm to 50 nm and a width in the range of 50 nm to 500 nm.

34. (New) The method of Claim 28 further comprising forming a metal channel with a plurality of layers.

35. (New) The method of Claim 28 further comprising forming the metal channel with a metal alloy, doped metal, metal silicide, metal salicide or metal nitride.